AMENDMENT UNDER 37 C.F.R. § 1.111
U.S. Appln. No. 10/662,380

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph 0034 with the following paragraph:

At a first time point t1 the input signal In is 1 and the state of the transparent D flip-flops is such that the lower transparent D flip-flop output B and the upper transparent D flip-flop output A is ~~1~~0. Since the clock Clk is 0 the transparent D flip-flop outputs A and B and the output Out do not change. When the clock Clk changes to 1 at the second time point t2, after a first delay d1, the transparent D flip-flop's latency, the output value B of the lower transparent D flip-flop is 1. The upper transparent D flip-flop output A remains on 0 since the input value Out of the upper transparent D flip-flop L1 did not change. At the third time point t3, the clock Clk falls on 0, ensuring that the outputs of the transparent D flip-flops are stable; the upper transparent D flip-flop output A is 0, the lower transparent D flip-flop output is 1. Then, after a second delay d2, the gate latency, the exclusive or gate produces a 1 at the output Out.